20V P-Ch Power MOSFET

V_{DS}		-20	V
$R_{DS(on),typ}$	V_{GS}=4.5V	5.6	mΩ
$I_{D\ (Sillicon\ Limited)}$		-46	A

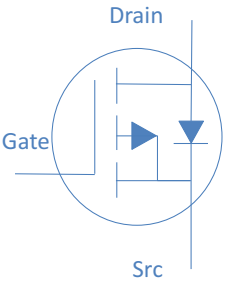
Feature

- High Speed Power Switching, Logic Level
- Enhanced Avalanche Ruggedness
- 100% UIS Tested, 100% Rg Tested
- Lead Free, Halogen Free

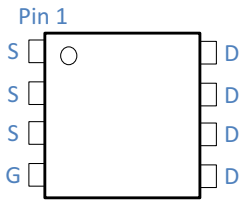
Application

- Hard Switching and High Speed Circuit
- DC/DC in Telecoms and Inductrial

DFN3x3



Part Number	Package	Marking
HTM063P02	DFN3*3	TM063P02



Absolute Maximum Ratings at T_j=25 (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_C=25	-46	A
		T_C=100	-29	
Drain to Source Voltage	V_{DS}	-	-20	V
Gate to Source Voltage	V_{GS}	-	±12	V
Pulsed Drain Current	I_{DM}	-	-180	A
Avalanche Energy, Single Pulse	E_{AS}	L=0.1mH, T_C=25	115	mJ
Power Dissipation	P_D	T_C=25	21	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to150	

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	50	/W
Thermal Resistance Junction-Ambient (steady state)	$R_{\theta JC}$	6	/W

Electrical Characteristics at T_j=25 (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value min	Value typ	Value max	Unit
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=-250μA	-20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=-250μA	-0.4	-0.6	-1.2	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=-16V, T_j=25	-	-	-1	μA
		V_{GS}=0V, V_{DS}=-12V, T_j=125	-	-	-10	
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±12V, V_{DS}=0V	-	-	±100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=-4.5V, I_D=-20A	-	5.6	6.3	mΩ
		V_{GS}=-2.5V, I_D=-20A	-	6.7	7.5	
		V_{GS}=-1.8V, I_D=-20A	-	8.4	9.5	
		V_{GS}=-1.5V, I_D=-20A	-	11.5	15	
Transconductance	g_{fs}	V_{DS}=-5V, I_D=-20A	-	52	-	S
Gate Resistance	R_G	V_{GS}=15mV, V_{DS} =0V, f=1MHz	-	3.3	-	Ω

Dynamic Characteristics

Input Capacitance	C_{iss}		-	6945	-	
Output Capacitance	C_{oss}	V_{GS}=0V, V_{DS}=-10V, f=1MHz	-	605	-	pF
Reverse Transfer Capacitance	C_{rss}		-	515	-	
Total Gate Charge	Q_g		-	49	-	
Gate to Source Charge	Q_{gs}	V_{DD}=-10V, I_D=-20A, V_{GS}=-4.5V	-	10	-	nC
Gate to Drain (Miller) Charge	Q_{gd}		-	7.6		

Reverse Recovery Time	t					ns
Reverse Recovery Charge	Q_{rr}		-			

Fig 1. Typical Output Characteristics

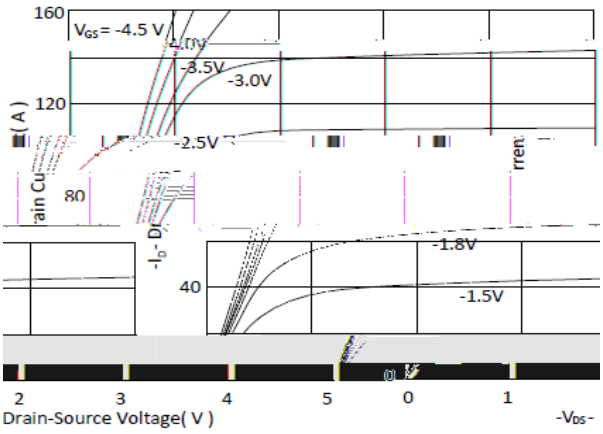


Figure 2. On-Resistance vs. Gate-Source Voltage

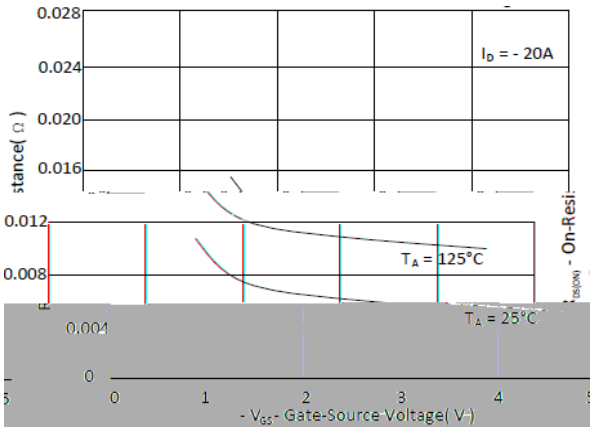


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

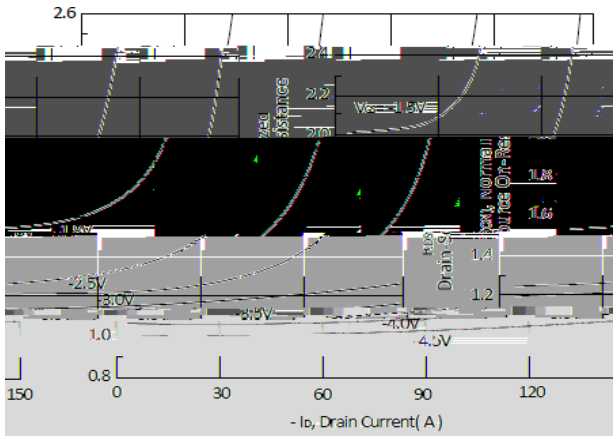


Figure 4. Normalized On-Resistance vs. Junction Temperature

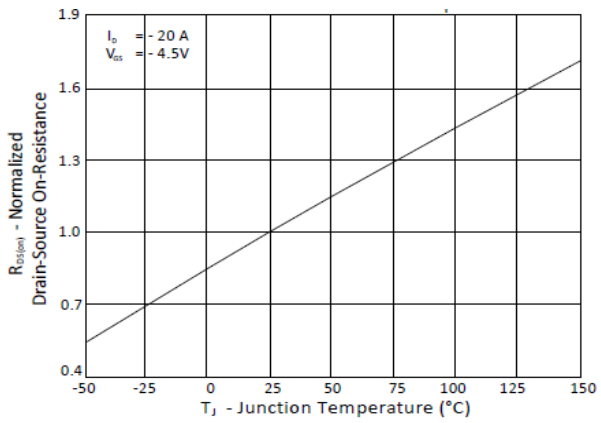


Figure 5. Typical Transfer Characteristics

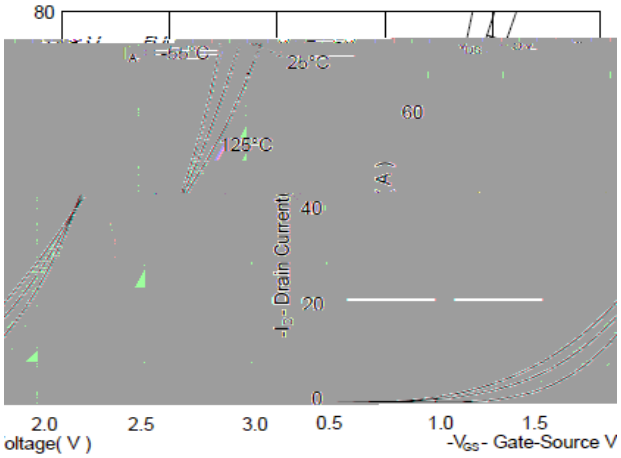


Figure 6. Typical Source-Drain Diode Forward Voltage

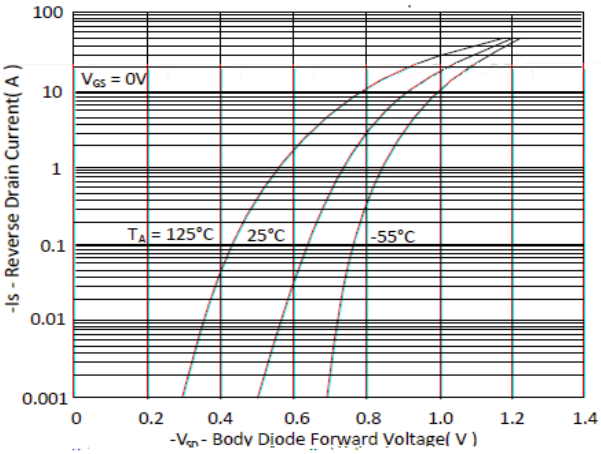


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

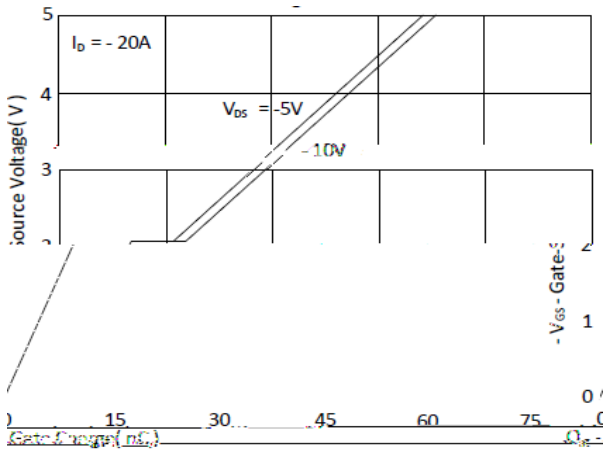


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

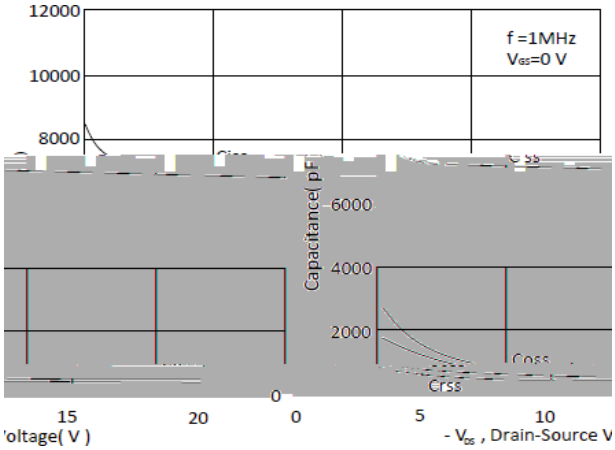


Figure 9. Maximum Safe Operating Area

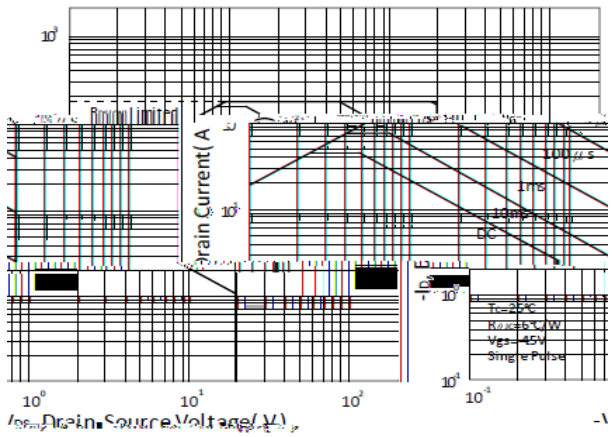


Figure 10. Single Pulse Maximum Power Dissipation

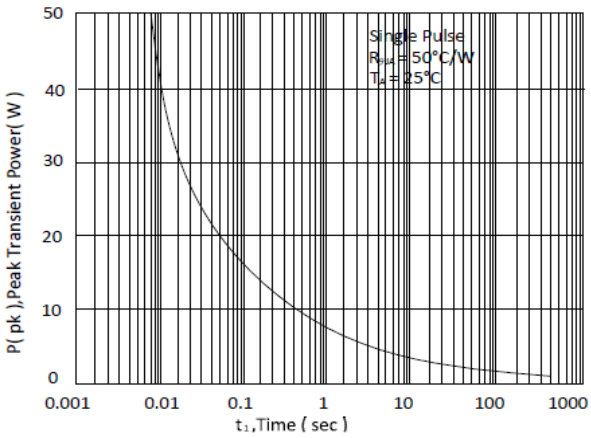
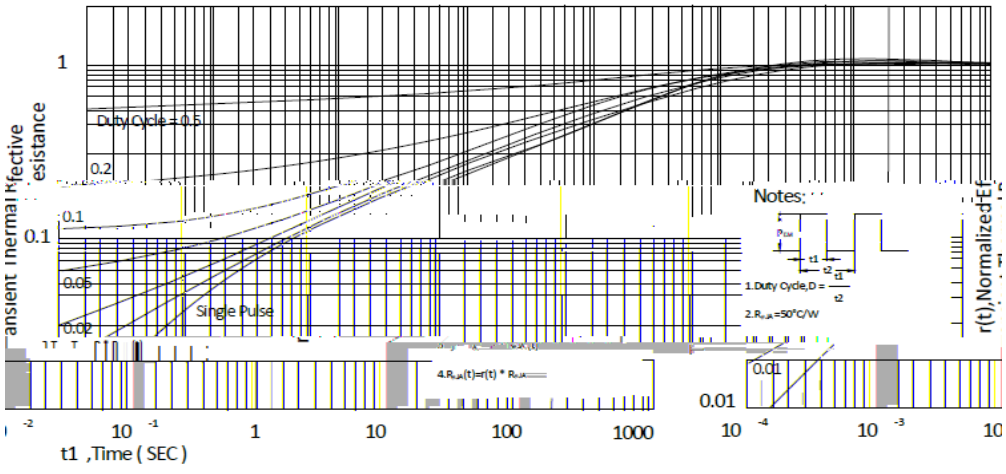
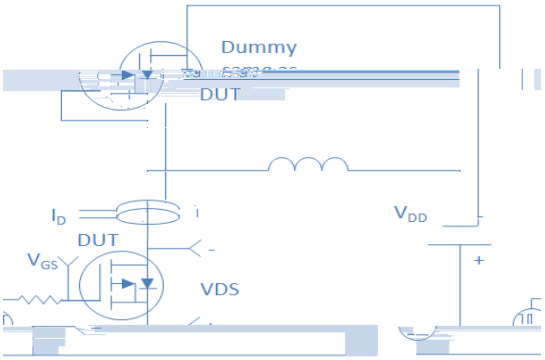
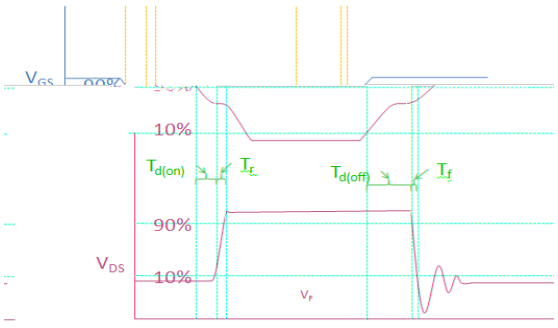


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient

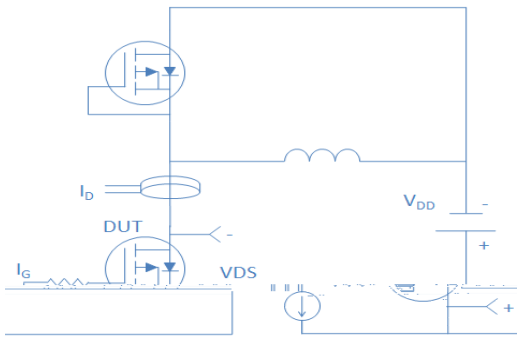


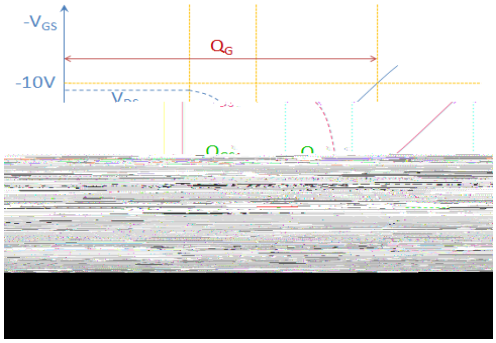
Inductive switching Test



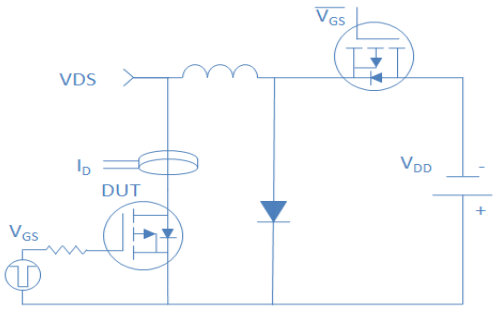


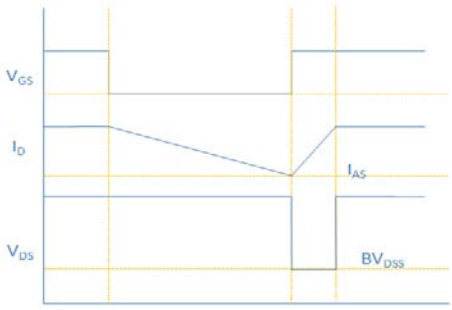
Gate Charge Test



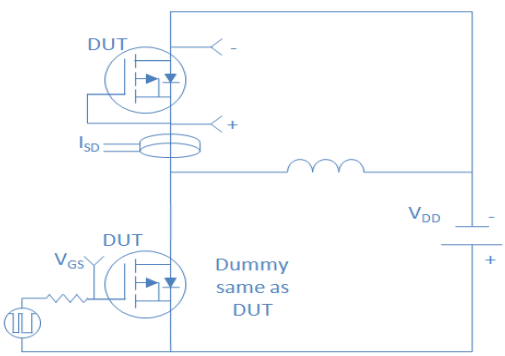


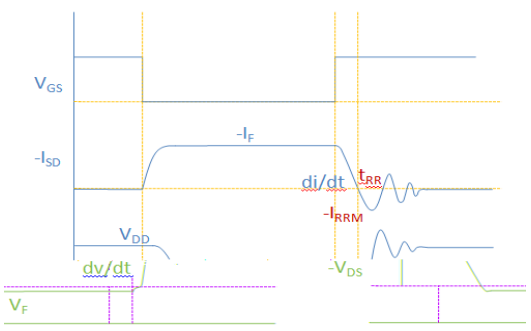
Uclamped Inductive Switching (UIS) Test





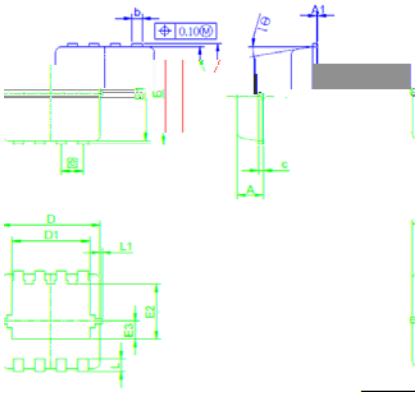
Diode Recovery Test





Package Outline

DFN3*3_P, 8leads



Dimension in mm

Dimension	A	A1	b	c	D	D1	E	E1	E2	E3	e	L	L1	θ1
Min.	0.70	0	0.24	0.10	2.95	2.25	3.15	2.95	1.65			0.30		0°
Typ.	0.80		0.30	0.152	3.00	2.35	3.30	3.00	1.75	0.575	0.65	0.40	0.13	10°
Max.	0.90	0.05	0.37	0.25	3.15	2.45	3.40	3.15	1.96			0.50		10°